FLEXIBLE BUFFERING SCHEME FOR MULTI-RATE SIMD PROCESSOR

ABSTRACT OF THE DISCLOSURE

A single instruction, multiple data (SIMD) architecture for controlling the processing of plurality of data streams in a digital subscriber line (DSL) system has a memory for storing the data from the channels, a processor operatively coupled with the memory for processing data from the data streams, and a controller for controlling the processor. Storing the data in the memory de-couples the operating rate of the processor and the operating rate of the data streams.